1. (Currently Amended) In the transmission of clocked time binary information signals with respect to a single reference level in a single information channel where said binary information signals are positioned between beginning and end phase shift signals,

an improvement for extraction of said phase shift signals comprising in combination:

means for arranging said binary information signals in serial relation to first, second and third voltage levels in said clocked time increments wherein each binary information signal is in two of said three voltage levels, such that there is a change in voltage level at every system clock cycle, said change in voltage level being correlated with logic and that there is a change every clock cycle which permits clock information from binary data bit voltage level information, said binary data then being reconstructed between precise levels and with subsequent precision timing and pulse shape, and

means for producing a new signal for each of said binary information signals that is based on an amplitude of a signal of said binary information signals that is greater than a low threshold that is less than the transition between said first and said second of said voiltage levels and is less than a high threshold that is greater than the transition between said second and said third voltage levels.

2. (Previously presented) The improvement of claim 1 wherein said means for arranging said binary information signals in serial relation to said first, second and third voltage levels includes a three level driver.

3. (Currently Amended) The improvement of claim ~~1~~ 2 wherein said means for producing a new signal for each of said binary information signals that is based on an amplitude of a signal that is greater than a low threshold that is less than the transition between said first and said second of said voltage levels and is less than a high threshold that is greater than the transition between said second and said thrid voltage levels as one reference and said low threshold as the other reference level.

4. (Previously presented) The improvement of claim ~~1~~ 3 wherein said means for producing a new signal includes means for reflecting "current" and "previous" data in relating said new signal to said clocked time.

5. (Previously Presented) The improvement of claim 4 wherein said means for electing "current" and "previous" data is a look-up table with said "previous" data provided from said "current" data with a one clock time cycle delay.

6. (Currently Amended) Clocked time binary information processing comprising:
the arrangement of said binary information signals in serial relation to first, second and third voltage levels in said clocked time increments wherein each binary information signal is in two of said three voltage levels, such that there is a change in voltage level at every system clock cycle, said change in voltage level being correlated with logic and that there is a change every clock cycle which permits clock information from binary data bit voltage level information, said binary data then being reconstructed between precise levels and with subsequent precision timing and pulse shape, and

~~the~~ producing ~~of~~ a new signal for each of said binary information signals that is based on an amplitude of a signal of said binary information signals that is greater than a low threshold that is less than the transition between said first and said second of said voiltage levels and is less than a high threshold that is greater than the transition between said second and said third voltage levels and the processing of said new signal in a differential amplifier between said high and said low threshold values.

7. (Curently Amended) The clocked time binary information processing of claim 6 including ~~the~~ an additional step of further position processing of said new signal with respect to said clocked time.

8. (Curently Amended) The clocked time binary information processing of claim 7 wherein said additional step is a signal positioning of said new signal at the leading edge of said clocked time.

9. (Currently Amended) The removal of clock timing information and signal reshaping in binary data comprising the steps of :
arranging said binary data in serial binary bits,
passing each bit in relation to first, second and third voltage levels, wherein each binary bit signal extends into two of said voltage levels such that there is a change in voltage level at every system clock cycle, said change in voltage level being correlated with logic and that there is a change every clock cycle which permits clock information from binary data bit voltage level information, said binary data then being reconstructed between precise levels and with subsequent precision timing and pulse shape, and

producing a new signal for each bit that is within an amplitude range that is greater than a low threshold value that is less than a transition value between said first and said second of said voltage levels and is less than a high threshold value greater than the transition value between said second and said third voltage levels, and,

positioning said new signal in relation to the leading edge of the next clock timing signal.

10. (Currently Amended) Data transmission apparatus for the transmission of binary data bits between first and second nodes, comprising in combination:

an input stage operable to receive a binary information signal at a first transmission node, said input stage being adapted to deliver a three voltage level driver signal ~~voltage~~ at an intermediate circuit node,

said three voltage level driver signal having serially, in a first clock cycle increment, a first voltage level corresponding to the system reference voltage,

in a second clock cycle increment, a second and intermediate~~[,]~~ voltage level and,

in a third clock cycle increment corresponding to a third and highest voltage level,

a comparator stage wherein said three level driver signal is compared in separate parallel first and second reference voltage comparison amplifiers each having said three level driver signal introduced at one input thereto;

a first reference voltage comparison amplifier having introduced at the remaining input a low threshold voltage that is higher than said reference voltage and is less than said intermediate voltage, and,

a second reference voltage comparison amplifier having introduced at the remaining input a high threshold voltage that is higher than said intermediate voltage and is less than said third voltage; and

a binary information signal reconstruction stage responsive to output signals from said first and second comparison amplifiers ~~ans~~ and adapted to establish the shape of an output binary bit signal;

such that there is a change in voltage level at every system clock cycle, said change in voltage level being correlated with logic and that there is a change every clock cycle which permits clock information from binary data bit voltage level information, said binary data then being reconstructed between precise levels and with subsequent precision timing and pulse shape.

11. The data transmission apparatus of claim 10 wherein said reconstruction stage includes delay means to position said output signal with respect to a clock for said data transmission system.

12. (Previously presented) The data transmission apparatus of claim 11 wherein said reconstruction stage includes variable delay means to position said output signal within a window established by said clock for said data transmission system.

13. (Previously presented) The data transmission apparatus of claim 12 wherein said reconstruction stage includes bistable circuit means establishing output signal turn-on.

14. (Presently Amended) The data transmission apparatus of claim ~~12~~ 13 wherein said reconstruction stage produces a new signal, the magnitude of which is within an amplitude range that is greater than a low threshold value that is less than an intermediate voltage value that is between said first and said second of said voltage levels, and is less than a high threshold value that is greater than said intermediate voltage, and, positioning said new signal in relation to the leading edge of the next clock timing signal.

15. (New) In the transmission of clocked time binary information signals with respect to a single reference level in a single information channel where said binary information signals are positioned between beginning and end phase shift signals,

an improvement for extraction of said phase shift signals comprising in combination:

means for arranging said binary information signals in serial relation to first, second and third voltage levels in said clocked time increments wherein each binary information signal is in two of said three voltage levels, such that there is a change in voltage level at every system clock cycle, said change in voltage level being correlated with logic and that there is a change every clock cycle which permits clock information from binary data bit voltage level information, said binary data then being reconstructed between precise levels and with subsequent precision timing and pulse shape, and

means for producing a new signal for each of said binary information signals that is based on an amplitude of a signal of said binary information signals that is greater than a low threshold that is less than the transition between said first and said second of said voltage levels and is less than a high threshold that is greater than the transition between said second and said third voltage levels, said means including means for reflecting "current" and "previous" data in relating said new signal to said clocked time; and said means for reflecting "current" and "previous" data is a look-up table with said "previous" data provided from said "current" data with a one clock time cycle delay.

16 (New) Data transmission apparatus for the transmission of binary data bits between first and second nodes, comprising in combination:

an input stage operable to receive a binary information signal at a first transmission node, said input stage being adapted to deliver a three voltage level driver signal at an intermediate circuit node,

said three voltage level driver signal having serially, in a first clock cycle increment, a first voltage level corresponding to the system reference voltage,

in a second clock cycle increment, a second and intermediate voltage level and,

in a third clock cycle increment corresponding to a third and highest voltage level,

a comparator stage wherein said three level driver signal is compared in separate parallel first and second reference voltage comparison amplifiers each having said three level driver signal introduced at one input thereto;

a first reference voltage comparison amplifier having introduced at the remaining input a low threshold voltage that is higher than said reference voltage and is less than said intermediate voltage, and,

a second reference voltage comparison amplifier having introduced at the remaining input a high threshold voltage that is higher than said intermediate voltage and is less than said third voltage; and

a binary information signal reconstruction stage responsive to output signals from said first and second comparison amplifiers and adapted to establish the shape of an output binary bit signal; such that there is a change in voltage level at every system clock cycle, said change in voltage level being correlated with logic and that there is a change every clock cycle which permits clock information from binary data bit voltage level information, said binary data then being reconstructed between precise levels and with subsequent precision timing and pulse shape;

said binary information reconstruction stage includes: (a) delay means to position said output signal with respect to a clock for said data transmission system; (b) variable delay means to position said output signal within a window established by said clock for said data transmission system and (c) bistable circuit means establishing output signal turn-on.